Report of MERIT internship (domestic)

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D2・MERIT 10th
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Company: Toshiba Electronic Devices & Storage Corporation

Research theme: The observation and simulation of parasitic oscillations in paralleled SiC power MOSFETs

The research during the internship

In terms of the high breakdown voltage and the low power loss, SiC power devices significantly outperform the conventional Si devices. Benefited from these outstanding features, SiC power devices are usually applied to higher speed switching devices. At the same time, in order to control high voltage and current, in general, SiC power devices are paralleled in the circuits. However, the high-speed switching and the inevitable unbalance in parasitic inductance of paralleled circuits may easily lead to a parasitic oscillation between paralleled devices. This oscillation emerges an instantaneous high voltage and current which excess the absolute maximum ratings of device and may result in an irreversible destruction to the devices. In this regard, for the design of SiC power devices, it is important to understand the origin of this parasitic oscillation and know how to avoid it. This time, for the paralleled SiC power MOSFET devices, we investigated the parasitic oscillation using both experimental and simulation approaches.

In the experimental approach, in order to monitor the voltage and current of each device simultaneously, an evaluation board loading discrete SiC power MOSFET was designed. As a result of switching experiment, intense oscillations were observed during the switch-off process. In addition, by controlling the device and circuit parameters, it is confirmed that the higher voltage, the higher current, the larger mutual conductance g_m, the larger extra gate resistance, and the difference in electrical characteristics between devices lead to more intense oscillation.

In the simulation approach, firstly, to represent the parasitic oscillations, SPICE simulations were employed. In order to replicate the experiment setting, before SPICE simulations, the parasitic components of the evaluation board and the package of MOSFET were evaluated by a parasitic extraction tool called “Ansys Q3D Extractor”, and the electrical characteristics of MOSFET were modeled by optimizing the model in Toshiba based on the measured characteristics. After modeling, the circuit was constructed and simulated on LTSpice. As a result, the parasitic oscillation with similar frequency and the same device parameter dependency were represented. By controlling the drain current and drain voltage, the phase diagram of the parasitic oscillation was created.

After SPICE simulation, to reveal the physics of the oscillation, a small signal analysis was performed to the low side MOSFETs, which is thought to be the origin of the parasitic oscillation. In the small signal analysis, an oscillation mode with a similar frequency was determined from the Bode plot, and the stability of this mode was analytically judged by the Nyquist stability criterion and the Hurwitz stability criterion. The phase diagram of the stability has a similar shape to the phase diagram obtained from the SPICE simulation, indicating this small signal analysis is an effective tool to understand the parasitic oscillations.

Impression

In the university, my research field is based on the academically interests, and the results of my research may not be applied to industry immediately. Therefore, in this internship, my goal is to experience the research for creating products, and also the one related to the semiconductor industry that I am interested in. This time, the division that I belonged to is in charge of the design of SiC power MOSFET. But the obligation is not only limited to the design, but also includes the reliability of chip and the evaluation of circuits with MOSFETs. Especially, the evaluation of circuits and the customers requests are important to develop the next design strategy. Indeed, my research theme is the part of the evaluation of circuits with MOSFETs, and the results will feedback to the design of MOSFET. Besides, the department, which contains the division that I belonged to, holds divisions in charge of process, package, mass production, and reliability, respectively, which is necessary for the development of a semiconductor product. In this department, the research and development do not rely on individual. Every step is moved forward by the cooperation of multiple divisions or people. This feature is so different from the research in university and impressed me very much. The experience of this internship will undoubtedly benefit to my future career selection and job hunting.

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